IN THE CLAIMS

Please amend the claims as follows:

1. (previously presented) A method for providing quality control of a wafer manufacturing line, said method comprising:

measuring resistances on a plurality of manufacturing test structures within a wafer running on a wafer manufacturing line;

obtaining an actual distribution value based on the result of said measured resistances on said plurality of manufacturing test structures;

recording the difference between said actual distribution value and a predetermined distribution value, wherein said predetermined distribution value is obtained based on a ground rule resistance;

measuring resistances on a plurality of design test structures within said wafer;

correlating said measured resistance of said design test structures to said measured resistance of said manufacturing test structures to obtain an offset value; and

adjusting resistances of an adjustable resistor circuit within said wafer and subsequent wafers running on said wafer manufacturing line according to said offset value.

2. cancelled

3. (original) The method of Claim 1, wherein said method further includes monitoring manufacturing test structures on wafers on said wafer manufacturing line.

4. (original) The method of Claim 3, wherein said method further includes adjusting resistances of an adjustable resistor circuit within a wafer on said wafer manufacturing line according to said offset value if the resistance of said manufacturing test structures on said wafer falls within a target resistance range.

5. (original) The method of Claim 4, wherein said method further includes discarding a wafer if the resistance of said manufacturing test structures on said wafer does not fall within said target resistance range.

6. (previously presented) A wafer testing system for providing quality control of a wafer manufacturing line, said wafer testing system comprising:

means for measuring resistances on a plurality of manufacturing test structures within a wafer running on a wafer manufacturing line;

means for obtaining an actual distribution value based on the result of said measured resistances on said plurality of manufacturing test structures;

means for recording the difference between said actual distribution value and a predetermined distribution value, wherein said predetermined distribution value is obtained based on a ground rule resistance;

means for measuring resistances on a plurality of design test structures within said wafer;

means for correlating said measured resistance of said design test structures to said measured resistance of said manufacturing test structures to obtain an offset value; and

means for adjusting resistances of an adjustable resistor circuit within said wafer and subsequent wafers running on said wafer manufacturing line according to said offset value.

7. cancelled

8. (original) The system of Claim 6, wherein said system further includes means for monitoring manufacturing test structures on wafers on said wafer manufacturing line.

9. (original) The system of Claim 8, wherein said system further includes means for adjusting resistances of an adjustable resistor circuit within a wafer on said wafer manufacturing line according to said offset value if the resistance of said manufacturing test structures on said wafer falls within a target resistance range.

10. (original) The system of Claim 9, wherein said system further includes means for discarding a wafer if the resistance of said manufacturing test structures on said wafer does not fall within said target resistance range.

11. (currently amended) A computer readable medium having computer program product for providing quality control of a wafer manufacturing line, said computer readable medium ~~program product~~ comprising:

program code means for measuring resistances on a plurality of manufacturing test structures within a wafer running on a wafer manufacturing line;

program code means for obtaining an actual distribution value based on the result of said measured resistances on said plurality of manufacturing test structures;

program code means for measuring resistances on a plurality of design test structures within said wafer;

program code means for correlating said measured resistance of said design test structures to said measured resistance of said manufacturing test structures to obtain an offset value; and

program code means for adjusting resistances of an adjustable resistor circuit within said wafer and subsequent wafers running on said wafer manufacturing line according to said offset value.

12. (currently amended) The computer readable medium ~~program product~~ of Claim 11, wherein said computer readable medium ~~program product~~ includes program code means for recording the difference between said actual distribution value and a predetermined distribution value, wherein said predetermined distribution value is obtained based on a ground rule resistance.

13. (currently amended) The computer readable medium ~~program product~~ of Claim 11, wherein said computer readable medium ~~program product~~ further includes program code means for monitoring manufacturing test structures on wafers on said wafer manufacturing line.

14. (currently amended) The computer readable medium ~~program product~~ of Claim 13, wherein said computer readable medium ~~program product~~ further includes program code means for adjusting resistances of an adjustable resistor circuit within a wafer on said wafer manufacturing line according to said offset value if the resistance of said manufacturing test structures on said wafer falls within a target resistance range.

15. (currently amended) The computer readable medium ~~program product~~ of Claim 14, wherein said computer readable medium ~~program product~~ further includes program code means for discarding a wafer if the resistance of said manufacturing test structures on said wafer does not fall within said target resistance range.